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IMPLEMENTATION OF VLSI ARCHITECTURE FOR RECONFIGURABLE RRC FIR FILTER USING GRAPH BASED METHOD

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ABSTRACT

The essential factors which contributes for designing the architecture of reconfigurable pulse shaping FIR filter are low complexity and power consumption. Although several low complexity architectures have been used for the optimization of Multiple Constant Multiplication (MCM), ie., the multiplication of a data sample by set of constants, further improvement in area and power consumption for RRC FIR filter design can be accomplished by employing the highly efficient algorithms. Hence the Graph Based (GB) algorithm had been implemented in RRC FIR filter. These GB methods are not limited to any particular number representation such as CSD, MSD, Binary and it yields better solutions than shift add implementation of constant multiplication. It is also capable of operating for different wordlength filter coefficients without any expense over the hardware circuitry. Hence it has been observed from the experimental result that the architecture using GB algorithm offers efficient area reduction and power consumption when compared to existing reconfigurable implementations using BCSE algorithm.

KEYWORDS: Multiple Constant Multiplication (MCM), Root Raised Cosine (RRC), Binary Common Subexpression Elimination (BCSE), Graph Based (GB) Algorithm

INTRODUCTION

FIR filter plays a vital role in the emerging wireless communication and DSP applications. The reduced bandwidth is required for this application. On the other side when rectangular pulses are passed through the band limited channel, the pulses spread with respect to time. So the pulses of each symbol will smear with succeeding symbols to form Inter Symbol Interference. To overcome ISI, larger channel bandwidth is required. Tackling these two contrary requirements at the same time leads to the development of RRC filters.

The most crucial part in the architecture of RRC FIR filter is shift and add unit.Hence, the multiplications of filter coefficient with the input data are generally implemented under shift and add architecture for its reduction in hardware. This normal shift and add implementation leads to the inclusion of maximum number of operations in the gate level design of the filter. To overcome that distinctive methods are there to implement the constant multiplication.

A straight way of implementing the shift and add architecture [1] involves the constant be first converted into binary. For each binary representation, the occurrence of shifts is done according to that particular bit position. This method is called digit based recoding. Depending on the number of non-zero digits present, the number of adders will be required for the product. So this method is useful for optimization of constant multiplication, but it is not optimal. Sign digit representations (SD) [2] are employed to optimize the multiple constant multiplication problems. One of the SD method is Canonic sign digit representation [3] which increases the number of zeros and inhibits the possibility of having two adjacent non zero digits. But, this representation does not contribute to give the minimum number of operations in MCM. Because, it uses single representation of a constant with minimum number of non-

zero digits and both positive, negative signs in the CSD representation may produce partial terms which are less common in the implementation of constants.

Other algorithms for the optimizing the number of operations in MCM can be categorized into two classes namely common subexpression elimination techniques and graph based techniques. Common Subexpression elimination (CSE) [4] algorithm is to finding the most common digit patterns in the set of constants multiplying a variable. CSD based CSE algorithm (CSD-CSE) [5] is used to identify the multiple occurrences of bit patterns that occur within the CSD representation of coefficients and eliminate the redundant multiplication. CommonSubexpression Elimination algorithm depends on number representation such as Binary. It is then named as Binary Common Subexpression Elimination algorithm (BCSE). In BCSE [6], redundant binary common subexpressions are eliminated by reusing the Binary Common Subexpressions that occur within the coefficients. The BCSE technique provides improved adder reductions and low complexity FIR filters when compared to CSD-CSE methods. The objective function for most of the MCM algorithm is to minimize the adder cost. The Graph Based Algorithm is proposed where the representation is not dependent. It produces the solution with minimum number of operations while compared to other techniques.

ARCHITECHTURE OF ROOT RAISED COSINE FIR FILTER (RRC FIR)

The RRC FIR filter architecture [8] plays a vital role in three communication standards namely universal mobile telecommunication, wideband code division multiple access and digital video broadcasting for its ability to reduce the bit error rate by not allowing the timing jitter at the sampling instant.

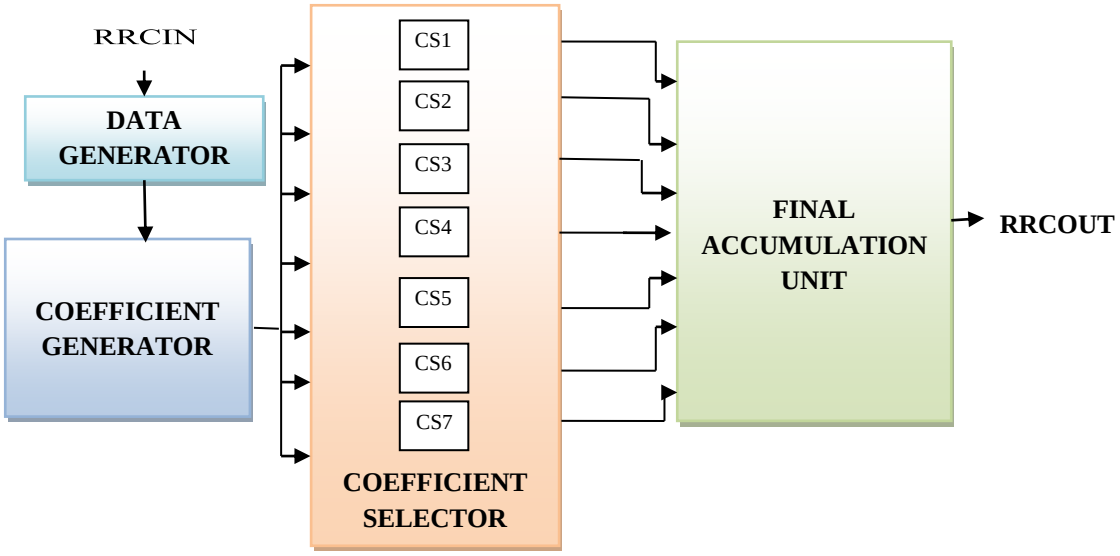

Fig.1 Architecture of RRC FIR filter

A. Data generator block (GB)

The interpolation factor for the universal mobile telecommunication standard be 4 for 25 tap filter, 8 for 49 tap filter, 16 for 97 tap filter. Depending upon the interpolation factor, the data generator block samples the input data sequence RRCIN and generates subfilter required for the different tap filters such as 25,49,97. For example, if 25 tap filter is used then the sub filters required for their implemenation be 25/4 ie., seven subfilters .

B. Coefficient generator block (CG)

The coefficient generator block performs the multiplication operation between the inputs and filter coefficients. The two stage optimisation technique is used in this CG block for simplifying the RRC FIR filter with lowest computation time and with low complexity. The flow diagram of the CG Block is shown in Fig.2 and its functionality is described as follows.

i) First Coding Pass (FCP)

For N tap filter with interpolation factor L requires (N/L) number of convolution operations and also it needs the number of structural adders for the addition operation. If M, N, O tap filter with interpolation factor L, P, Q requires large number of convolution operations and more structural adders for their implementation. Henceforth for a constant propagation delay, the area and power consumption increases with rise in number of multipliers and structural adders. For this, the optimization is done by First coding Pass (FCP) block. In this FCP, filters varying only by the filter parameters are passed through the 2:1 multiplexer where the control parameter called rolloff factor selects the desired filter.

ii) Second Coding Pass (SCP)

The selected filter coefficients from the First Coding Pass block are passed through the second coding pass block. Depending on the interpolation factor, filter coefficients are coded accordingly.

iii) Shift and Add Unit

Then the multiplication operation performs between the input data and filter coefficients selected from Second Coding Pass (SCP). For Partial product generation Binary Common Subexpression Elimination Technique (BCSE) is used for eliminating the most common subexpressions within the coefficients

iv) Multiplexer Unit

The multiplexer unit selects the output generated from the shift and add block depending upon the coded coefficients.

v) Addition Unit

The addition operation can be performed by summing all the outputs of partial product generator followed by eight multiplexer units.

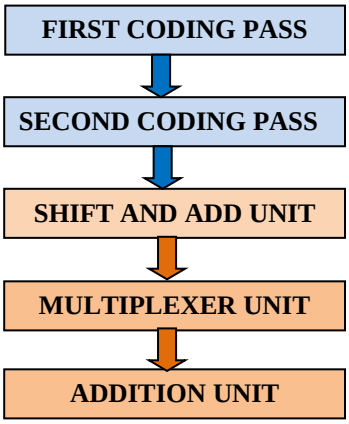

Fig.2 Coefficient Generator

C. Coefficient selector block

The proper data from the coefficient generator block is steered to final accumulation unit according to the interpolation factor parameter.

D. Final data accumulation unit

The reconfigurable pulse shaping FIR filter is based on transposed direct form architecture.

BINARY COMMON SUBEXPRESSION ELIMINATION (BCSE) ALGORITHM

BCSE [7] deals with the elimination of redundant Binary Common Subexpressions (BCSs) that occur within the coefficients. The BCSE technique targets on eliminating redundant computations in coefficient multipliers by reusing the most common binary bit patterns (BCSs) present in coefficients. An n-bit binary number can form $2^n - (n + 1)$ BCSs among themselves. For example, a 2-bit binary representation can form only one BCS, which is "11". These BCSs can be expressed as [1 1] = x1 = x+ 2^{-1}x where x is the input signal. The other representation such as 00, 01 and 10 does not require adder for the implementation as they have zero and only one non zero bit is available. The straightforward implementation of the above BCS requires only one adder.The number of adders required for all the possible n-bit binary subexpressions is $2^{n-1} - 1$. For n=3, the number of adders required are three. For n=2, the

number of adders needed are one. The number of adders needed for the implementation of coefficient multipliers using BCSE [7] is considerably less than the CSD-based CSE methods.

GRAPH BASED ALGORITHM

The proposed technique implemented in the architecture of RRC FIR is graph based algorithm. These algorithms are not restricted to any particular number representation and it will synthesize the constants by building a graph. This graph based algorithm consists of two parts. They are optimal part and heuristic part. In optimal part, the target constant can be implemented in single operation, whose inputs are in the ready set.

In another part called heuristic, if there exists unimplemented elements in the target set whose inputs are not in the ready set, then the algorithm moves to this part where an intermediate constant is added to the ready set for reaching the target set value. Hence this exact algorithm finds the minimum number of intermediate constants and finds the minimum number of operations solution for the implementation of architecture.

A. Implementation of GB Algorithm

In the proposed graph based algorithm, there will be ready set and target set. Initially ready set always be 1, the target coefficient values are to be fixed. The target set elements must be made odd and positive integer. To reach the target set coefficients from ready set, the intermediate constants must be needed. The intermediate constant must also be odd and positive integer. The generation of intermediate constant depends upon the bit-width of the filter.

For example, if bit-width=3, then the intermediate constant range is from 1 to 15 which is based on j=1 to 2^{bw+1}-1. According to this algorithm, after the synthesis of optimal part if there exist unimplemented constants in the target set then the synthesis of heuristic part will gets started using the intermediate constant. The processing of each intermediate constant with the target set iteratively selects the best intermediate constant. By using this intermediate constant, the partial products of target constants are shared and the number of operations for shift and add unit will be gets reduced. For example if target set T = {39, 53, 7, 11, 9, 13} then the shift and add implementation using graph based algorithm is shown in Fig.3. The figure describes one sub tractor and five adders are required for the implementation of target set with six filter coefficients

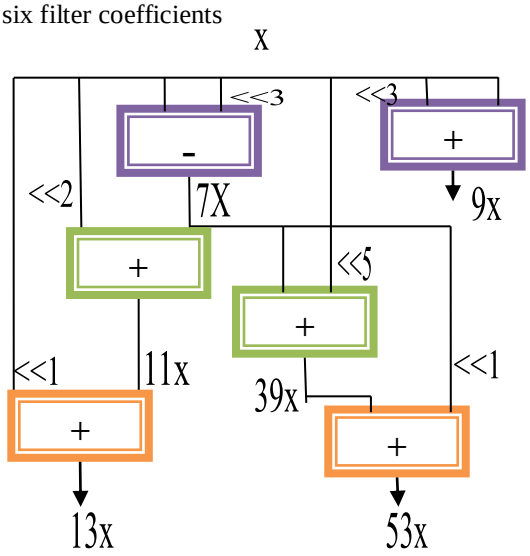

Fig3. Implementation of target constants using GB algorithm

Henceforth this GB algorithm has been adopted in the above coefficient generator block as described in Fig.2 for its optimization in area and power. Then the carry save adder is used in the addition unit of coefficient generator block for increase in the gate level speed of constant multiplication in RRC FIR filter.

RESULTS AND DISCUSSION

Simulation has been done in Xilinx ISE design 14.2 for synthesizing purposes. Then the synthesized filter design is implemented in Xilinx's SPARTRAN 3E FPGA. The results depicted in Fig.4 describes that the architecture of RRC FIR filter using BCSE algorithm has 68.4% improvement in the LUT consumption and 39% improvement in the speed. From Fig.5, it has been proven that the proposed architecture using GB algorithm provides 28% more gate consumption and also be noticed that the speed be improved by 58.3% than the previously used BCSE algorithm. Fig.6 describes the comparison of power in terms of mw and Fig.7 shows that the speed of implementing the architecture using GB is faster when compared to BCSE algorithm.

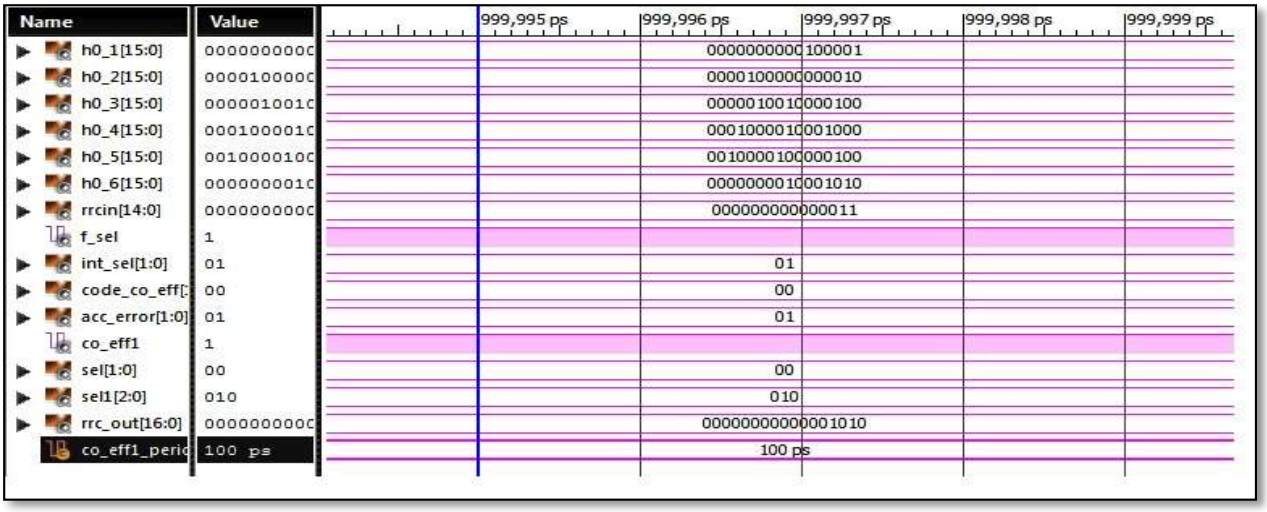

Fig.4Simulation result of BCSE algorithm for optimization of MCM design

Fig.5 Simulation result of RRC FIR filter architecture using graph based algorithm

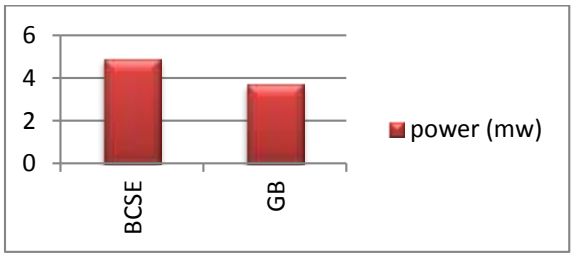

Fig.6 Comparison of power in terms of mw

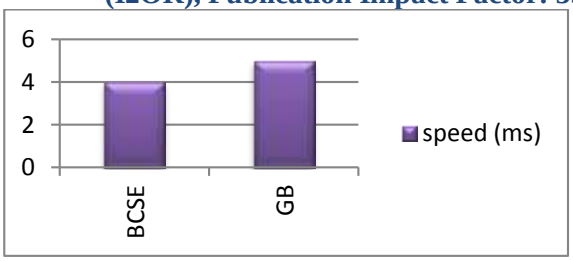

Fig.7 Comparison of speed in terms of ms

CONCLUSION

The observations of experimental result states that the design of MCM operation in the shift and add architecture with the use of Graph Based algorithm achieves significant area reduction and power consumption with respect to filter design where the multiplier part is implemented by using BCSE algorithm. The implementation of RRC FIR filter design in FPGA demonstrates the merits of proposed architecture in terms of area and power. Also it is recommended that the proposed design will be remarkably suited for next generation multistandard communication systems.

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